FPGA Lab

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Physics 315

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Open the ISE project Navigator

File - > New Project

Give your project a name with no spaces or special characters. DON’T USE hyphens! (-)

Under top-level source choose HDL

Click next

Under evaluation development board choose Spartan 6 sp601 evaluation platform

Product category family speed package will all be chosen for you

Under Preferred language choose VHDL

Click next

You will get a project summary window (new project 4.png)

This closes the new project wizard, and dropes you into your ISE project navigator Integrated Development enviroment. It is a very non-intuitive interface, that you will only become accustom to with experience.

We will be building a simple And circuit using VHDL and manual schematic layouts. Both are achieve the same thing, although VHDL will eventually get you more mileage.

Add a new source schematic to your project by selecting Project -> New Source which oopens the new source wizard (new source wizard 1)

Give it a name, avoiding special characters and click next to get to the summary of the wizzarrd ( new source wizard 2)

Click finished

It will create the schematic and open it. (new schematic 1)

Click the add symbol toolbar button in the vertical toolbar strip

This opens a menu to the left of the toolbar with digital electronic components. They are sorted into categories for somewhat quick access, but the name filter is the quickest way to find what you are looking for if you know the name

Click the logic category, and notice the symbols list shortened to only show the logic componants in alphabetical oder

Choose the and2 symbole from the symbol menu.

Now when you roll over the schematic view, you get something that looks like that compotant following around a cross. This lets you know what symbol you are holding and ready to place on your schematic. (schematic placement)

Go ahead and place two of these and gates, by hovering to where you want to place them, and clicking once . Press escape to clear your placement selection and go back to mouse mode. (schematic placed).

To see more clearly, lets zoom in. Use the zoom tools to zoom in on your parts. (zoom.png) or the zoom select tool from the verticle menu.

Use the add wire tool in the verticle toolbar to add short wires to the three leads on your and gate. Clicking on the terminal on the and gate, then clicking where you want the wire to go drops a wire segment. Double clicking will end the wireplacement. Press escape to end wireplacement all together and clear your tool. (add wire tool)

Add IO markers. These markers wire your circuit to the inputs and outputs of your fpga.

Click the add IO button in verticle tool bar. Click all 3 terminal leads to drop a marker. (lead marker dropped).

Right click to rename each port. Name the inputs A and B and the output OUT1 (io rename)

Check your schematic for errors in Tools -> Check shematic (check schematic png)

Errors show up in the conosole at the bottom. Fix any errors.

File -> Save all

Now we test our schematic to see if it works.

Project -> Add Source

Select VHDL Test Bench

Give it a name and press next (addtb)

The next window will ask you to select wich vhdl or schematic to test

You only have one (AND\_schematic) so select that (tbconfirm)

Click next to view a summary (tbsummary)

The wizard will close and you will be presented with a file called [name of file].vhd which is your vhdl code you will use to specify how to test your schematic you slected in the wizard..